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# UTILITY PATENT APPLICATION TRANSMITTAL
## (Large Entity)

*(Only for new nonprovisional applications under 37 CFR 1.53(b))*

Docket No.
12906 (YO999-358)

Total Pages in this Submission
3

**TO THE ASSISTANT COMMISSIONER FOR PATENTS**
**Box Patent Application**
**Washington, D.C. 20231**

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

**SILICATE GATE DIELECTRIC**

and invented by:

**Eduard Albert Cartier**
**Matthew Warren Copel**
**Frances Mary Ross**

**If a CONTINUATION APPLICATION,** *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

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Enclosed are:

**Application Elements**

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having **twenty-two (22)** pages and including the following:
   a. ☒ Descriptive Title of the Invention
   b. ☒ Cross References to Related Applications *(if applicable)*
   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   d. ☐ Reference to Microfiche Appendix *(if applicable)*
   e. ☒ Background of the Invention
   f. ☒ Brief Summary of the Invention
   g. ☒ Brief Description of the Drawings *(if drawings filed)*
   h. ☒ Detailed Description
   i. ☒ Claim(s) as Classified Below
   j. ☒ Abstract of the Disclosure

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**Application Elements (Continued)**

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☐ Formal Number of Sheets _____
   b. ☒ Informal Number of Sheets five (5)
4. ☒ Oath or Declaration
   a. ☒ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☒ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
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   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

**Accompanying Application Parts**

8. ☒ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS Citations
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**Accompanying Application Parts (Continued)**

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☒ Additional Enclosures *(please identify below):*

**Executed Appointment of Associate Power of Attorney and Request for Change of Mailing Address**

**Fee Calculation and Transmittal**

**CLAIMS AS FILED**

| For | #Filed | #Allowed | #Extra | | Rate | Fee |
|---|---|---|---|---|---|---|
| **Total Claims** | 34 | - 20 = | 14 | x | $18.00 | $252.00 |
| **Indep. Claims** | 3 | - 3 = | 0 | x | $78.00 | $0.00 |
| **Multiple Dependent Claims (check if applicable)** ☐ | | | | | | $0.00 |
| | | | | | **BASIC FEE** | $760.00 |
| **OTHER FEE *(specify purpose)*** | **Recordation of Assignment** | | | | | $40.00 |
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*Signature*

Dated: **October 6, 1999**

**Richard L. Catania, Reg. No.: 32,608**
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**(516) 742-4343**

cc:

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Invention: **SILICATE GATE DIELECTRIC**



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# SILICATE GATE DIELECTRIC

## DESCRIPTION

## RELATED APPLICATIONS

This application is related to U.S. application, Serial No. 08/431,349, filed April 28, 1995 by R.B. Laibowitz, et al., entitled "Lead Silicate Based Capacitor Structures."

## Field of the Invention

The present invention relates to a method of fabricating silicate dielectrics that have superior electrical properties compared with $SiO_2$ and to semiconductor structures such as field effect transistors (FETs) which contain the same.

## Background of the Invention

In the field of semiconductor transistor manufacturing, the formation of a gate dielectric is a critical step in the fabrication process. It is highly desirable in such art to reduce the leakage current that is caused by electron tunneling through the $SiO_2$ layer conventionally used as the gate dielectric.

One approach to improving the electrical characteristics of the gate dielectric is to use an alternative dielectric material with a larger dielectric constant

than $SiO_2$; allowing the use of a greater physical thickness for the gate insulator.

Numerous transition metal oxides have larger dielectric constants than $SiO_2$; however maintaining compatibility with standard silicon processing is a tremendous challenge.

A complete discussion on the above compatibility problem is provided by K.J. Hubbard, et al. "Thermodynamic Stability of Binary Oxides in Contact With Silicon," J. Mater. Res., Vol. 11, No. 11, pp. 2757-2776 (1996).

There is thus a need for developing a method of fabricating dielectric materials having dielectric constants greater than $SiO_2$ which maintain compatibility with standard silicon processing. There is also a need for developing a method of fabricating dielectric materials in which the electrical properties of the dielectric are superior to $SiO_2$ dielectrics heretofore known.

## Summary of the Invention

One object of the present invention is to provide a method of fabricating a dielectric material which maintains compatibility with standard silicon processing.

Another object of the present invention is to provide a method of fabricating a dielectric material having a dielectric constant greater than $SiO_2$.

A further object of the present invention is to provide a method of fabricating a dielectric material which can significantly reduce the leakage current normally associated with an $SiO_2$ dielectric.

A yet further object of the present invention is to provide a simple method of forming a silicate/$SiO_2$ gate stack with a self-limiting oxide equivalent thickness.

These and other objects and advantages are obtained in the present invention by oxidizing a metal oxide layer that is formed on a silicon substrate under conditions sufficient to convert the metal oxide layer into a silicate by intermixing with the underlying silicon, while simultaneously oxidizing the underlying silicon. Specifically, the method of the present invention comprises the steps of:

(a) forming a metal oxide layer on a silicon-containing material; and

(b) heating the metal oxide layer in the presence of an oxidizing agent under conditions so as to convert the metal oxide layer into a metal silicate layer while simultaneously oxidizing a portion of the silicon-containing material underlying the metal silicate layer.

In one embodiment of the present invention, the method of the present invention further comprises annealing the metal silicate layer produced in step (b) above.

In yet another embodiment of the present invention, an elemental metal layer is formed on the silicon-containing material and thereafter step (b) is performed. In this embodiment, the oxidation step, step (b), is carried out under conditions that are effective in transforming the metal layer to a metal oxide layer and then to a metal silicate layer.

Another aspect of the present invention relates to semiconductor structures such as capacitors and transistors which include at least the metal silicate produced by the method of the present invention therein. Specifically, the inventive semiconductor structures comprise at least a metal silicate that is formed on a silicon oxide layer, said silicon oxide layer being formed on a Si-containing substrate.

Another aspect of the present invention relates to a field effect transistor which comprises a Si-containing semiconductor substrate;

spaced apart source and drain regions in said substrate, said spaced apart source/drain regions defining a channel region;

a dielectric layer above said channel region, said dielectric layer including a first layer of a metal silicate; and

a gate electrode formed over said dielectric layer.

## Brief Description of the Drawings

Figs. 1a-b illustrate cross-sectional views of a structure during different processing steps of the present invention (1a prior to oxidation and 1b after oxidation).

Figs. 2a-b illustrate cross-sectional views of another structure during different processing steps of the present invention (2a prior to oxidation and 2b after oxidation).

Fig. 3 is a graph of ion yield vs. energy showing the effect of post-oxidation on a $La_2O_3/SiO_2/Si$ structure of the present invention.

Fig. 4 is a graph of ion yield vs. energy showing the effect of post-oxidation on a $ZrO_2/SiO_2/Si$ structure.

Figs. 5a-c are X-ray photoemission spectroscopy results for the formation of lanthanum silicate.

Fig. 6 is a cross-sectional TEM image of lanthanum silicate/$SiO_2$/Si(001) structure of the present invention.

Fig. 7 is a TEM diffraction pattern of a lanthanum silicate film of the present invention.

Fig. 8 is a graph of capacitance vs. gate biases for the inventive La silicate capacitor with Al contacts.

Fig. 9 is a graph illustrating the leakage current density for the inventive La silicate capacitor after conducting a forming gas anneal step.

## Detailed Description of the Invention

The present invention which provides a method for forming a metal silicate having superior electrical properties will now be described in greater detail by referring to the drawings that accompany the present application. It is noted that in the drawings like reference numerals are used for describing like and/or corresponding elements.

Reference is first made to Figs. 1a-1b and 2a-b which illustrate the basic processing steps that are employed in the present invention. Specifically, Fig. 1a shows a structure which comprises a silicon-containing material 10 and a metal oxide layer 12 formed on said silicon-containing material.

Suitable silicon-containing materials that can be employed in the present invention include conventional materials such as Si-containing semiconductor substrates, silicon-on-insulators, sapphire, $SiO_2$, SiGe, Si oxynitride or combinations thereof. The present invention also contemplates a layered substrate such as substrates containing layers of Si; Ge; SiGe and Si; SiGe, Si and Ge; and SiGe. A preferred silicon-containing material employed in the present invention is a Si-containing semiconductor substrate 11 having a thin layer 13 of $SiO_2$ or Si oxynitride formed thereon. Such a structure is shown in Fig. 2a. It is also possible to

employ a Si-containing substrate that has a native oxide layer located near the surface of the substrate or to employ a bare Si-containing substrate.

The semiconductor substrates employed in the present invention may contain source/drain regions, isolation regions and other like regions therein. For simplicity these regions are not shown in the drawings of the present invention, but nevertheless are intended to be within regions 10 or 11.

The thin layer of $SiO_2$ or Si oxynitride may be formed on the surface of the Si-containing semiconductor substrate using conventional thermal oxidation or by a suitable deposition process such as chemical vapor deposition, plasma-assisted chemical vapor deposition, evaporation, sputtering and other like deposition processes. The thickness of the oxide or oxynitride layer is typically of from about 0 to about 25 Å. As mentioned above, the $SiO_2$ layer may be a native oxide that is inherently present in the substrate, and in one embodiment of the present invention the native oxide may be removed prior to conducting step (a).

It is noted that when an oxide or oxynitride layer is present on the structure prior to oxidation, silicon from the layer will be consumed in forming the silicate. If the oxide or oxynitride layer is completely consumed, a new $SiO_2$ layer will be formed between the silicate and the substrate during the oxidation step of the present invention. In this sense, the growth is self-limiting; the thickness of the silicate is controlled by the amount

of metal oxide deposited, and the thickness of the underlying $SiO_2$ layer is controlled by the oxidation kinetics during the post-deposition oxidation step. If the preexisting oxide or oxynitride layer is sufficiently thick, then it will not be entirely consumed in the post-deposition oxidation step, and the preexisting $Si/SiO_2$ interface will remain intact.

Metal oxide layer 12 of the present invention comprises oxygen and at least one metal selected from the group consisting of La, Hf, Y, Sc, Sr, Ba, Ti, Ta, W, Cr, Ca, Mg, Be, Pr, Nd and any other transitional metal or rare earth metal that is capable of forming an oxide. The metals employed in the present invention must also be capable of intermixing with the underlying Si so as to form a metal silicate during oxidation treatment. Mixtures and alloys of one or more of these metals is also contemplated herein. Preferred metals include La, Hf and Y. Of those preferred metals, oxides of La such as $La_2O_3$ are most highly preferred in the present invention.

The metal oxide layer may be formed using conventional deposition processes well known to those skilled in the art including, but not limited to: chemical vapor deposition, plasma vapor deposition, evaporation, sputtering and other like deposition processes. It is also possible to employ a reactive deposition process wherein an elemental metal is deposited in the presence of an oxidizing gas ($O_2$, $N_2O$ or NO). In this case, the metal reacts with the oxidizing agent causing in-situ deposition of a metal oxide film.

In one embodiment of the present invention, instead of forming a metal oxide layer on the Si-containing material prior to oxidation, a layer comprising an elemental metal is formed on the Si-containing material. In this embodiment, the elemental metal may be one of the above-mentioned transition metals or rare earth metals. Any conventional deposition process is used in forming the metal layer which will be first converted into a metal oxide layer and then to a metal silicate during the oxidation step of the present invention.

The metal oxide or metal layer formed on the Si-containing material typically has a thickness of from about 1 to about 50 Å. More preferably, the thickness of the metal oxide or metal layer is from about 5 to about 25 Å. Other thicknesses are also contemplated herein.

In accordance with the next step of the present invention, structures Fig. 1a or 2a (or a structure containing an elemental metal layer) are then subjected to an oxidation step in which the metal layer (metal oxide or elemental metal) is heated in the presence of an oxidizing agent under conditions so as to convert the metal oxide into a metal silicate layer 14 while simultaneously oxidizing the silicon-containing material underlying the metal silicate forming $SiO_2$ layer 16. The formation of the metal silicate is believed to be caused by the intermixing of the metal oxide with the underlying silicon.

In the cases shown in Figs. 1b and 2b, the oxidation step of the present invention causes the formation of an

underlying $SiO_2$ layer 16. In the case wherein an elemental metal is deposited, the oxidation step results in the conversion of the metal layer into a metal oxide layer which in turn is converted to a metal silicate, while simultaneously forming an underlying $SiO_2$ layer beneath the metal silicate.

The oxidation step of the present invention is carried out at a temperature of less than about 950°C for a time period of at least about 10 seconds. More preferably, the oxidation step is carried out at a temperature of from about 750° to about 900°C for a time period of from about 60 to about 180 seconds.

The oxidizing agents employed in this step of the present invention include, but are not limited to: $O_2$, $N_2O$, NO or any other reactive gas which causes oxidation of the metal oxide layer. During oxidation, the pressure of the oxidizing agent is at least about $10^{-5}$ torr, with a pressure of from about $10^{-3}$ to about $10^{-2}$ torr being highly preferred. Other pressures are possible depending on the desired thickness of the metal silicate layer. Typically, in the present invention, the metal silicate has a thickness of from about 20 to about 50 Å, while the underlying $SiO_2$ layer formed during oxidation has a thickness of from about 5 to about 15 Å.

The present invention also contemplates using ion implantation or a layer providing a source of oxygen in place of the above mentioned oxidizing agents.

In one embodiment of the present invention, the structures shown in Figs. 1b or 2b may be subjected to a

post-oxidation annealing step. This optional anneal is carried out in a forming gas atmosphere or other suitable annealing atmosphere at a temperature less than about 700°C for a time period of greater than 1 second. More preferably, the optional anneal is carried out at a temperature of from about 350° to about 650°C for a time period of from about 10 seconds to about 1 hour.

After formation of the metal silicate layer, electrically conductive contacts (or gate electrodes) can be formed on the surface of the metal silicate and that structure can undergo conventional transistor/capacitor processing steps. Suitable electrically conductive contacts that can be employed in the present invention include, but are not limited to: polysilicon, W, Al or Pt.

When metal silicates of the present invention are used as a dielectric material, the structures containing the same have leakage currents below $1x10^{-4}$ amps/cm$^2$ at -1 volts and a capacitance density of greater than $9x10^{-6}$F/cm$^2$. Moreover, the metal silicates of the present invention have dielectric constants greater than $SiO_2$ (k=4). Typically, the metal silicates have dielectric constants of from about 10 to about 40. In view of these properties, the metal silicates of the present invention are viable replacements for $SiO_2$ dielectrics.

The following example is given to illustrate the present invention as well as to demonstrate some advantages that are obtained by using the same.

## EXAMPLE

In this example, a $La_2Si_2O_7$ dielectric film is formed using the method of the present invention. Specifically, a Si (100) substrate containing a 25 Å thick thermal oxide formed by $N_2O$ oxidation was used as the Si-containing semiconductor material. If the oxide surface was exposed to atmosphere prior to use, it can be heated in vacuum at 500°-600°C for between 10 minutes and 24 hours to reduce surface contamination.

A 20 Å thick layer of $La_2O_3$ was e-beam evaporated from a $La_2O_3$ target. The La oxide layer was then oxidized at 880°C in $6x10^{-3}$ torr of $O_2$ for about 2 minutes. Afterwards, the sample was treated by a forming gas anneal at 400°C for about 20 minutes.

This resulted in a metal silicate film having 40 Å of $La_2Si_2O_7$ on 13 Å of $SiO_2$, as measured by medium energy ion scattering. The oxide equivalent thickness (EOT) by C(V) measurements is 19 Å. Films with smaller EOT can be made by a combination of decreasing the thickness of the preexisting oxide, reducing the quantity of $La_2O_3$ deposited, and lowering the pressure during the post-deposition oxidation.

### Experimental Results

MEIS (medium energy ion scattering) spectra for films during various stages of processing are shown in Fig. 3. Deposition of a 20 Å thick $La_2O_3$ film on a 20 Å $SiO_2$ layer shifted the position of the Si peak below the expected position for surface Si. This is due to the energy loss

the ions experience in traversing the $La_2O_3$ layer to reach the $SiO_2$. With heating in $O_2$, the leading edge of the silicon signal processed towards high energies, reaching the position for surface Si after the 880°C oxidation. At this point, the silicate formation was complete, and the spectrum can be accurately modeled as a stoichiometric $La_2Si_2O_7$ layer.

The formation of a silicate layer is not obvious, since it does not occur for all metal oxides. For example, if $ZrO_2$ is substituted for $La_2O_3$, no silicate forms. This is shown in Fig. 4 where a 38 Å thick $ZrO_2$ layer on 8 Å of $SiO_2$ on Si(001) was used and was heated to 930°C in 0.1 torr of $O_2$. The underlying $SiO_2$ layer had grown thicker, but the Si and Zr had not intermixed to form a silicate.

Core-level photoelectron spectroscopy results showed that the $La_2O_3$ and Si formed a distinct silicate, rather than a mixture of phase separated components. Figs. 5a-c show x-ray photoelectron spectra for films in various stages of reaction. The O1s core line has a binding energy of 533.8eV for $SiO_2$. After $La_2O_3$ was deposited, two peaks are visible at 533 and 530.5 eV, the latter corresponding to the oxygen in the $La_2O_3$. When the sample was reacted, the oxygen levels combined to form a single peak at 532.1 eV. The shift in the oxygen core to a position in between the O-La and O-Si positions indicated that each oxygen atom has a O-Si and an O-La bond. This is only possible if a compound had formed. The shift is chemical in nature, because the $Si_{2s}$ core line at 151.4 due to the substrate remains unchanged when the reaction occurs. A shift in the $La_3d5/2$ peak towards higher binding energy was also observed as a result of silicate formation.

Examination of the films by transmission electron microscopy revealed that the silicate was microcrystalline in nature, having a diffraction pattern characterized by a series of rings (Fig. 7). From dark field imaging, it was established that the domain size was roughly 50 Å. Cross-sectional images confirmed that the film was composed of a bilayer, with the top layer consisting of denser material (Fig. 6). Given the MEIS results, it was reasonable to conclude that the darker region was the lanthanum silicate, and the lighter region was composed of $SiO_2$. The image also showed that the silicon-dielectric interface was flat, which is essential to carrier mobility in a FET.

Al contacts were evaporated onto the silicate layer for electrical measurements. The capacitance of the dielectric stack was equivalent to an oxide thickness of less than 20 Å (Fig. 8). The C(V) curves show a feature at -1.5V indicative of undesirable defect states. The feature was absent from samples that underwent a 400°C forming gas anneal. Leakage current measurements indicated that after a forming gas anneal, the leakage was $10^5$ less than would occur with an $SiO_2$ film with the same capacitance (Fig. 9).

While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and detail may be made without departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact

forms described and illustrated but fall within the scope of the appended claims.

## CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A method of forming a metal silicate layer in a semiconductor structure comprising the steps of:

(a) forming a metal oxide layer on a silicon-containing material; and

(b) heating said metal oxide layer in the presence of an oxidizing agent under conditions so as to convert the metal oxide layer into a metal silicate layer while simultaneously oxidizing a portion of the silicon-containing material underlying the metal silicate layer.

2. The method of Claim 1, wherein said metal oxide comprises oxygen and at least one metal selected from the group consisting of La, Hf, Y, Sc, Sr, Ba, Ti, Ta, W, Cr, Ca, Mg, Be, Pr, Nd and mixtures and alloys thereof.

3. The method of Claim 2, wherein the at least one metal is La, Hf or Y.

4. The method of Claim 1, wherein said metal oxide is $La_2O_3$.

5. The method of Claim 1, wherein an elemental metal layer is formed in place of the metal oxide layer

and step (b) converts said metal layer to a metal oxide layer and then to a metal silicate.

6. The method of Claim 1, wherein said silicon-containing material is a Si-containing semiconductor substrate, a silicon-on-insulator, sapphire, $SiO_2$, SiGe, Si oxynitride or any combination thereof.

7. The method of Claim 1, wherein said silicon-containing material comprises a Si-containing semiconductor substrate having an exposed $SiO_2$ surface layer.

8. The method of Claim 7, wherein said exposed $SiO_2$ surface layer is removed prior to conducting step (a).

9. The method of Claim 1, wherein said silicon-contained material is a layered material.

10. The method of Claim 1, wherein said metal oxide layer is formed by a deposition process selected from the group consisting of chemical vapor deposition, plasma-vapor deposition, sputtering, evaporation, reactive deposition and other like deposition processes.

11. The method of Claim 1, wherein said metal oxide layer has a thickness of from about 1 to about 50 Å.

12. The method of Claim 1, wherein step (b) is conducted at a temperature of less than about 950°C for a time period of at least about 10 seconds.

13. The method of Claim 12, wherein step (b) is conducted at a temperature of from about 750° to about 900°C for a time period of from about 60 to about 180 seconds.

14. The method of Claim 1, wherein said oxidizing agent comprises $O_2$, $N_2O$ or NO.

15. The method of Claim 1 further comprising annealing the metal silicate layer formed in step (b).

16. The method of Claim 15, wherein said annealing is carried out using a forming gas anneal.

17. The method of Claim 16, wherein said forming gas anneal is carried out at a temperature of less than about 700°C for a time period of greater than 1 second.

18. The method of Claim 17, wherein said forming gas anneal is carried out at a temperature of from about 350°C to about 650°C for a time period of from about 10 seconds to about 1 hour.

19. The method of Claim 1 further comprising forming an electrically conductive contact on the surface of said metal silicate.

20. The method of Claim 19, wherein said electrically conductive contact is polysilicon, W, Al or Pt.

21. A semiconductor structure comprising at least a metal silicate that is formed on a silicon oxide layer, said silicon oxide layer being formed on a Si-containing semiconductor substrate.

22. The semiconductor structure of Claim 21, wherein said metal silicate comprises at least a metal selected from the group consisting of La, Hf, Y, Sc, Sr, Ba, Ti, Ta, W, Cr, Ca, Mg, Be, Pr, Nd and mixtures and alloys thereof.

23. The semiconductor structure of Claim 22, wherein said metal is La, Hf or Y.

24. The semiconductor structure of Claim 21, wherein said metal silicate is a La silicate.

25. The semiconductor structure of Claim 21, wherein said silicon oxide layer has a thickness of from about 5 to about 10 Å.

26. The semiconductor structure of Claim 21, wherein said metal silicate has a thickness of from about 20 to about 50 Å.

27. The semiconductor structure of Claim 21, wherein said structure has a leakage current below 1 x $10^{-4}$ amps/$cm^2$ at -1 volts and a capacitance density of greater than 5x$10^{-6}$ F/$cm^2$.

28. A field effect transistor comprising:

a Si-containing semiconductor substrate;

spaced apart source/drain regions in said substrate defining a channel region therein;

a dielectric layer above said channel region, said dielectric layer including a first layer of a metal silicate; and

a gate electrode formed over said dielectric layer.

29. The field effect transistor of Claim 28, wherein said metal silicate comprises at least a metal selected from the group consisting of La, Hf, Y, Sc, Sr, Ba, Ti, Ta, W, Cr, Ca, Mg, Be, Pr, Nd and mixtures and alloys thereof.

30. The field effect transistor of Claim 29, wherein said metal is La, Hf or Y.

31. The field effect transistor of Claim 28, wherein said silicate is La silicate.

32. The field effect transistor of Claim 28, wherein said dielectric layer includes a layer of $SiO_2$ between said substrate and said layer of metal silicate.

33. The field effect transistor of Claim 28, wherein said gate electrode comprises polysilicon, W, Al or Pt.

34. A capacitor comprising at least the metal silicate obtained by Claim 1 sandwiched between the same or different electrode materials.

ABSTRACT OF THE DISCLOSURE

**SILICATE GATE DIELECTRIC**

A method of forming a silicate dielectric having superior electrical properties comprising forming a metal oxide layer on a Si-containing semiconductor material and reacting the metal oxide with the underlying Si-containing material in the presence of an oxidizing gas is provided. Semiconductor structures comprising the metal silicate formed over a $SiO_2$ layer are also disclosed herein.

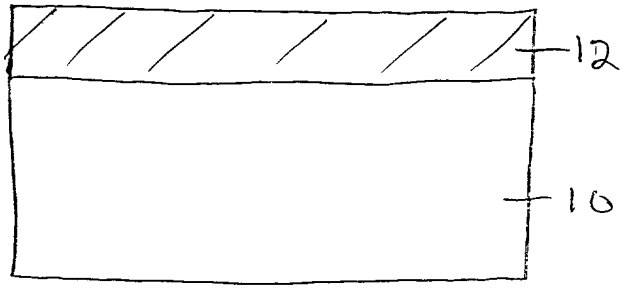



Fig. 1a

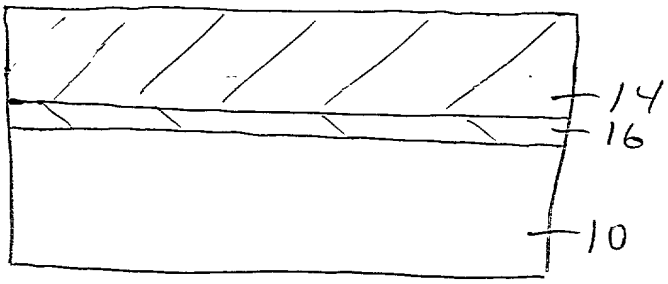



Fig. 1b

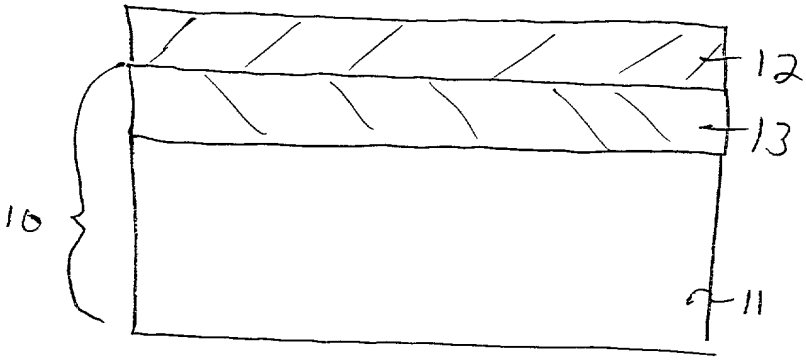



Fig. 2a

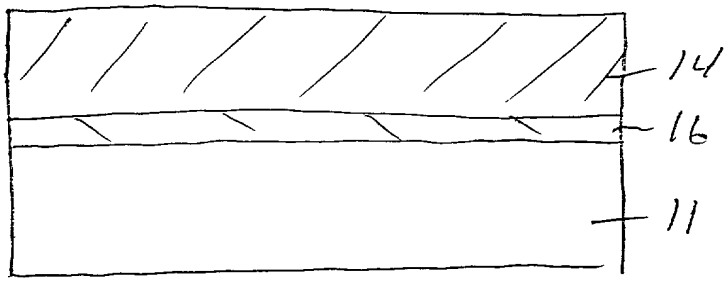

14
16
11

Fig. 2b

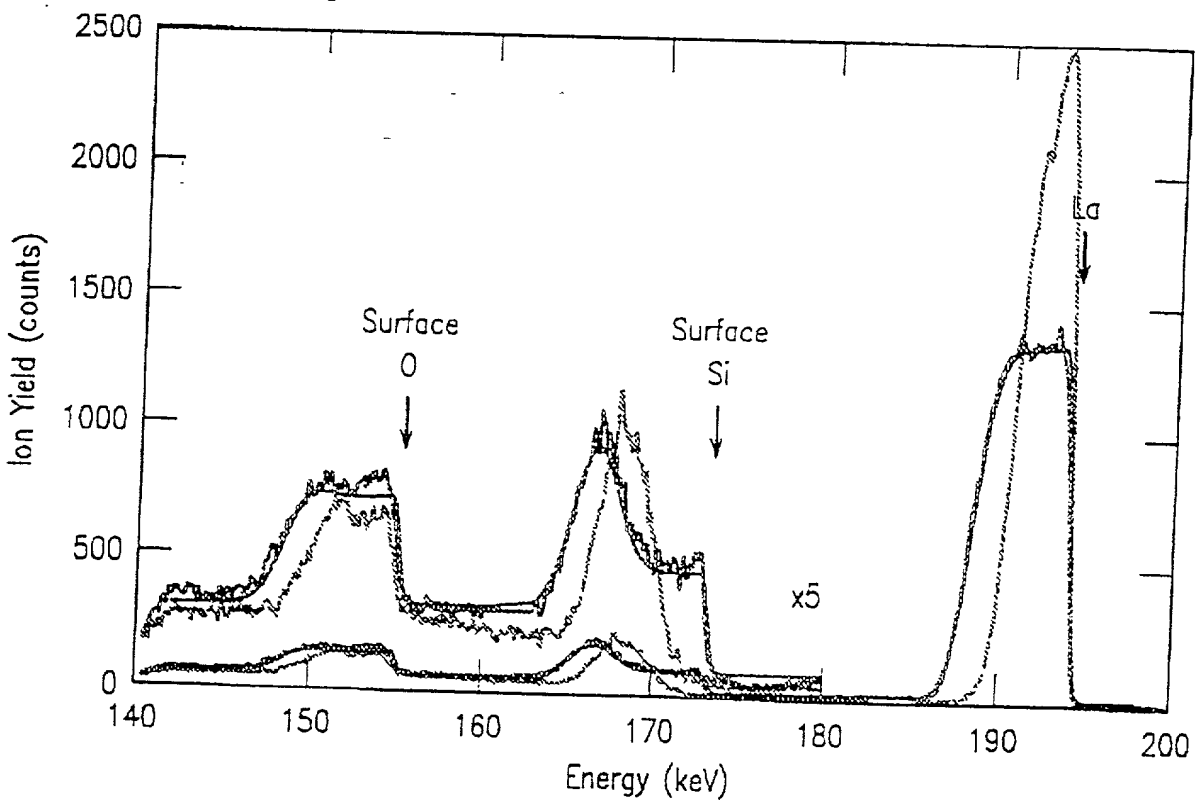

2500
2000
1500
1000
500
0
Ion Yield (counts)
Surface
O
Surface
Si
x5
a
140
150
160
170
180
190
200
Energy (keV)

Fig. 3

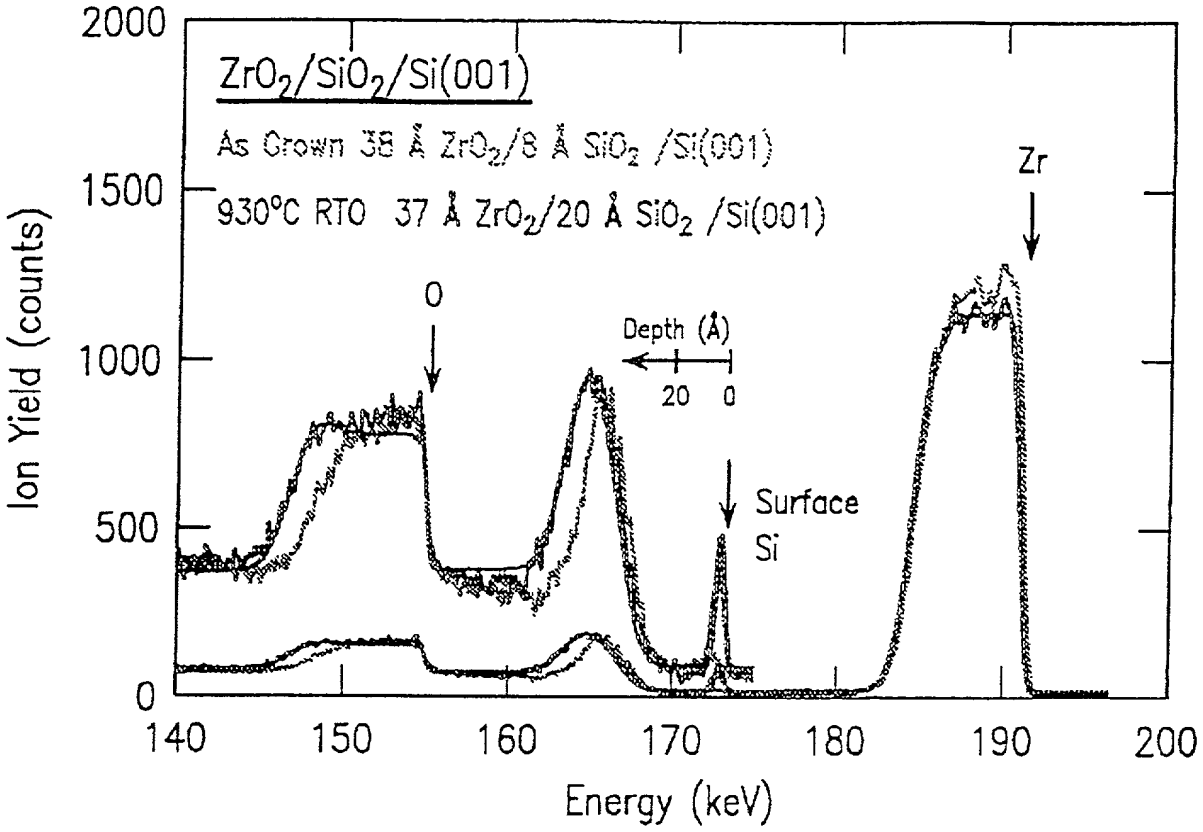
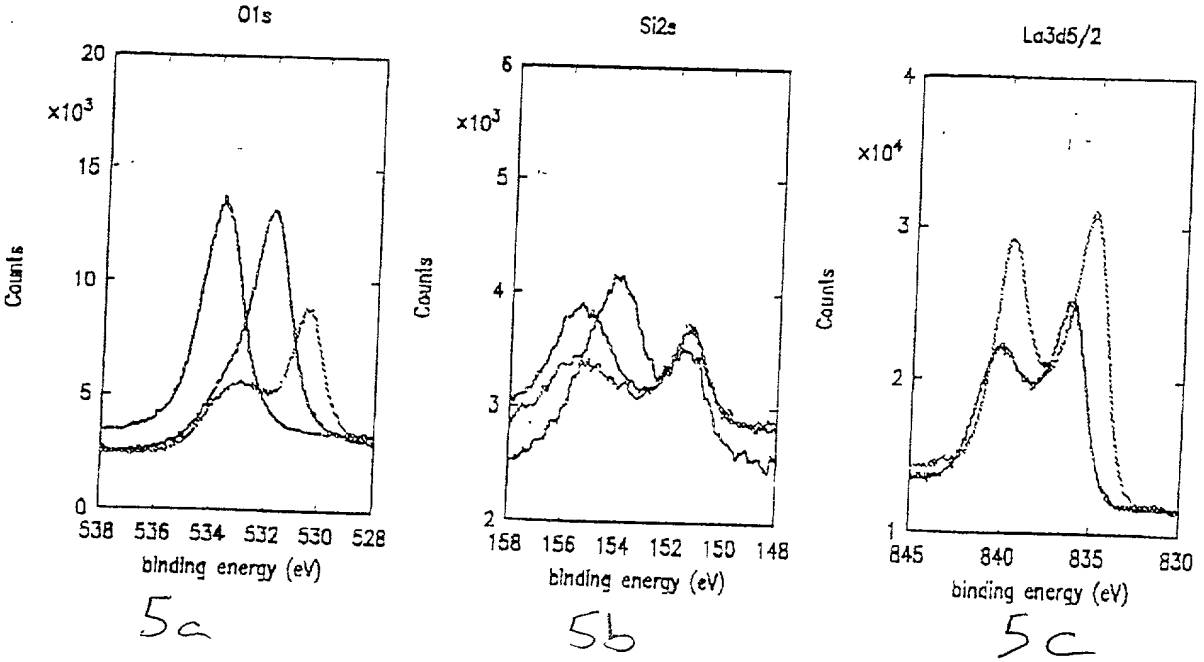

$ZrO_2/SiO_2/Si(001)$
As Grown 38 Å $ZrO_2$/8 Å $SiO_2$ /Si(001)
930°C RTO 37 Å $ZrO_2$/20 Å $SiO_2$ /Si(001)
Zr
O
Depth (Å)
20 0
Surface Si
Ion Yield (counts)
Energy (keV)
2000
1500
1000
500
0
140 150 160 170 180 190 200

Fig. 4


O1s
Si2s
La3d5/2
Counts
binding energy (eV)
×10³
×10⁴
538 536 534 532 530 528
158 156 154 152 150 148
845 840 835 830

5a 5b 5c

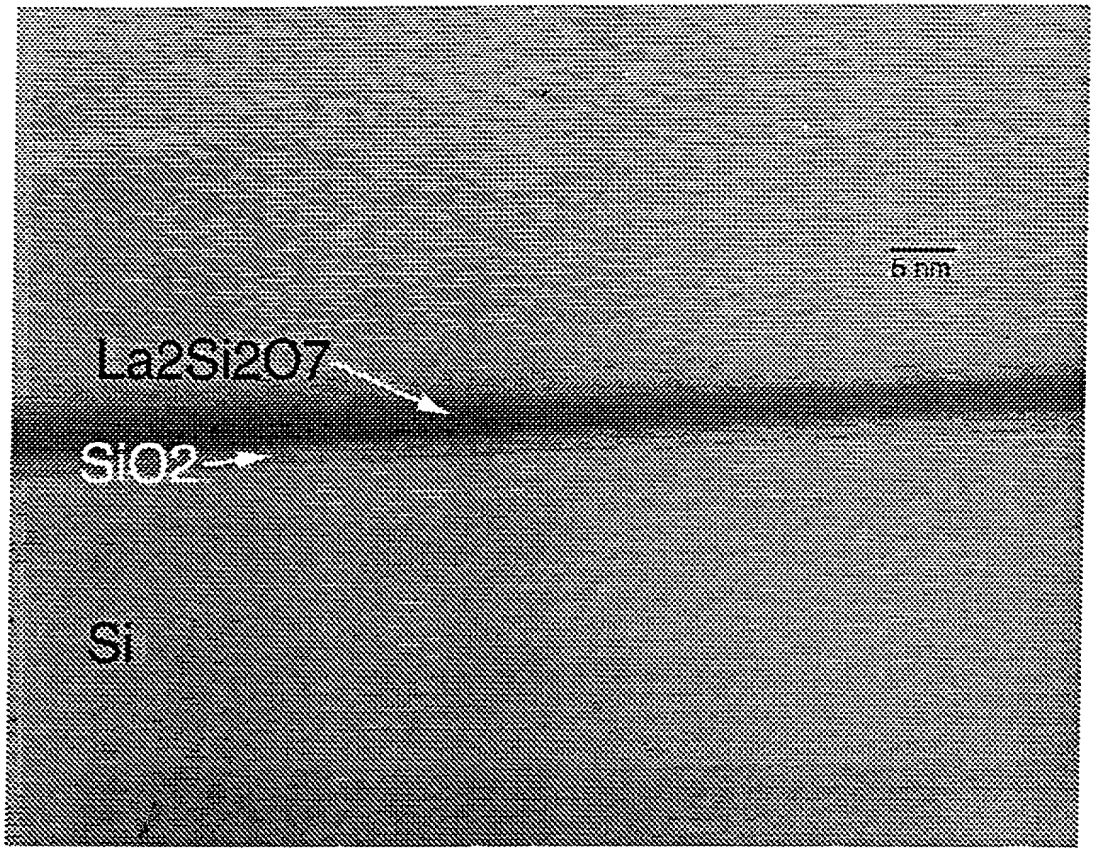



Fig 6

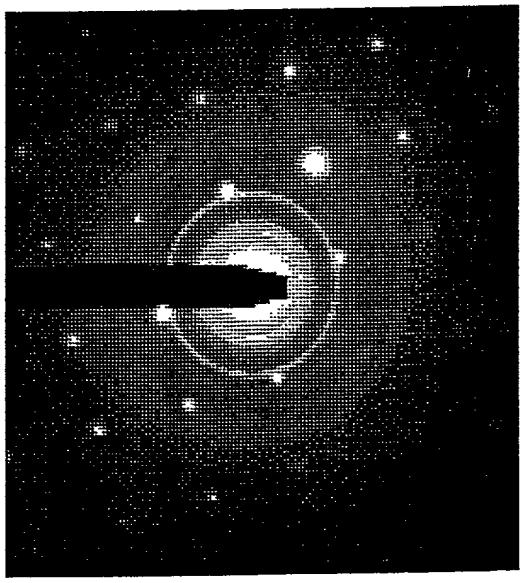


Fig. 7

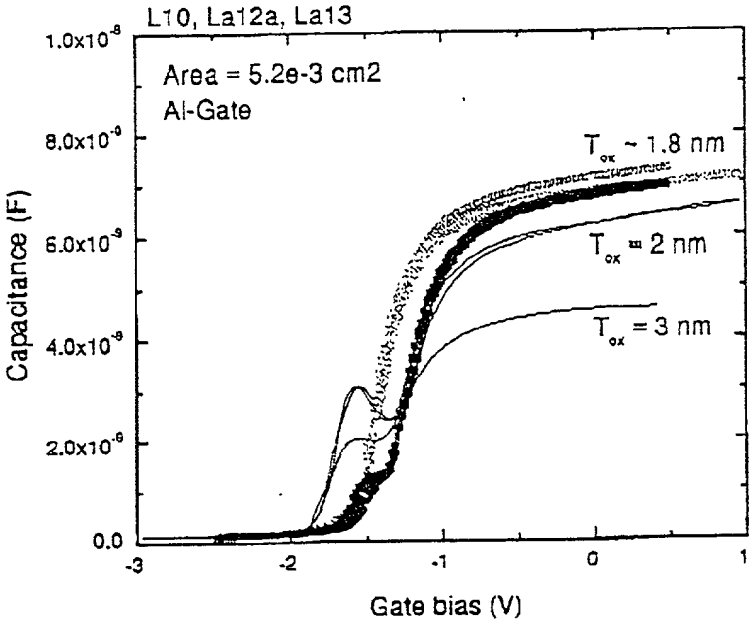

L10, La12a, La13
Area = 5.2e-3 cm2
Al-Gate
$T_{ox}$ ~ 1.8 nm
$T_{ox}$ = 2 nm
$T_{ox}$ = 3 nm
Capacitance (F)
1.0x10⁻⁸
8.0x10⁻⁹
6.0x10⁻⁹
4.0x10⁻⁹
2.0x10⁻⁹
0.0
-3
-2
-1
0
1
Gate bias (V)

Fig. 8

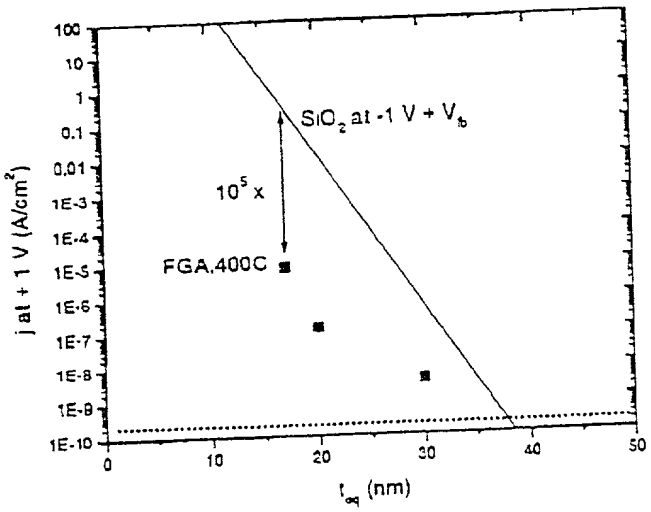

$SiO_2$ at -1 V + $V_{fb}$
$10^5$ x
FGA,400C
j at + 1 V (A/cm²)
100
10
1
0.1
0.01
1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
1E-10
0
10
20
30
40
50
$t_{ox}$ (nm)

Fig. 9

SSM&P Docket No.: 12906
IBM Docket No.: YO999-358

# DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SILICATE GATE DIELECTRIC

the specification of which (check one)

X is attached hereto.

___ was filed on _____ as United States Application Number _____

or PCT International Application Number _____

and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application, having a filing date before that of the application on which priority is claimed:

| Prior Foreign Application(s) | | | Priority Claimed |
|---|---|---|---|
| _____ (Number) | _____ (Country) | _____ (Day/Month/Year Filed) | ___ Yes ___ No |
| _____ (Number) | _____ (Country) | _____ (Day/Month/Year Filed) | ___ Yes ___ No |
| _____ (Number) | _____ (Country) | _____ (Day/Month/Year Filed) | ___ Yes ___ No |

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

| | |
|---|---|
| _____ (Application Number) | _____ (Filing Date) |
| _____ (Application Number) | _____ (Filing Date) |

I hereby claim the benefit under 35 U.S.C. §120 of any United States Application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States, or PCT International application in the manner provided by the first paragraph of 35 U.S.C. §112, I acknowledge the duty to disclose information material to the patentability of this application as defined in 37 CFR §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

| | | |
|---|---|---|
| _____ (Application Serial No.) | _____ (Filing Date) | _____ (Status) (patented, pending, abandoned) |
| _____ (Application Serial No.) | _____ (Filing Date) | _____ (Status) (patented, pending, abandoned) |

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number).

Manny W. Schecter (Reg. 31,722), Terry J. Ilardi (Reg. 29,936), Christopher A. Hughes (Reg. 26,914), Edward A. Pennington (Reg. 32,588), John E. Hoel (Reg. 26,279), Joseph C. Redmond, Jr. (Reg. 18,753), Douglas W. Cameron (Reg. No. 31,596), Kevin M. Jordan (Reg. No. 40,277), Stephen C. Kaufman (Reg. No. 29,551), Daniel P. Morris (Reg. No. 32,053), Paul J. Otterstedt (Reg. No. 37,411), Louis J. Percello (Reg. No. 33,206), Jay P. Sbrollini (Reg. No. 36,266), David M. Shofi (Reg. No. 39,835), Robert M. Trepp (Reg. No. 25,933) and Louis P. Herzberg (Reg. No. 41,500).

SSM&P Docket No.: 12906
IBM Docket No.: YO999-358

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Inventor's signature Date

Residence

Citizenship

Post Office Address

PATENTS

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Applicant(s):** Eduard Albert Cartier, et al. **Docket:** 12906 (YO999-358)

**Serial No.:** Unassigned **Dated:** X Oct. 1, 1999

**Filed:** Herewith

**For:** SILICATE GATE DIELECTRIC

Assistant Commissioner for Patents
Washington, DC 20231

**ASSOCIATE POWER OF ATTORNEY AND REQUEST FOR CHANGE OF MAILING ADDRESS**

Sir:

Applicants, by their attorneys of record, hereby grant an Associate Power of Attorney to:

RICHARD L. CATANIA, Reg. No. 32,608; FRANK S. DIGIGLIO, Reg. 31,346; KENNETH L. KING, Reg. No. 24,223; STEPHEN D. MURPHY, Reg. No. 22,002; LEOPOLD PRESSER, Reg. No. 19,827; JOHN S. SENSNY, Reg. No. 28,757; and EDWARD W. GROLZ, Reg. No. 33,705

with full power of substitution to prosecute this application and transact all business in the United States Patent and Trademark Office in connection therewith.

Applicants further request that all future correspondence in connection with this application be directed and addressed to:

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Respectfully submitted,

(date on top) X Robert M. Trepp

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